CLAIMS

What is claimed is:

1. A multi-chips stacked package, comprising:

a substrate having an upper surface, a lower surface and an opening passing through the upper surface and the lower surface;

an upper chip having a first active surface and a first back surface wherein the upper chip is flipped over and attached to the upper surface of the substrate via a plurality of electrically conductive bumps; and

a lower chip accommodated in the opening, disposed on the first active surface of the upper chip and electrically connected to the first active surface of the upper chip through a plurality of first electrically conductive wires.

2. The multi-chips stacked package of claim 1, further comprising a plurality of second electrically conductive wires connecting the second active surface of the lower chip and the lower surface of the substrate.

3. The multi-chips stacked package of claim 1, further comprising a dam located at the periphery of the opening and on the lower surface of the substrate.

4. The multi-chips stacked package of claim 3, wherein the dam is formed in a ring-like shape.

5. The multi-chips stacked package of claim 3, wherein the dam is made of an epoxy.

6. The multi-chips stacked package of claim 1, further comprising an underfill covering the electrically conductive bumps.

7. The multi-chips stacked package of claim 1, further comprising an encapsulation

covering the electrically conductive bumps, the first electrically conductive wires, the lower chip and the upper chip.

8. The multi-chips stacked package of claim 1, further comprising an adhesive layer interposed between the first active surface of the upper chip and the second back surface of the lower chip.

9. The multi-chips stacked package of claim 1, further comprising a plurality of solder balls formed on the lower surface of the substrate.

10. The multi-chips stacked package of claim 1, wherein the upper chip covers the opening.

11. The multi-chips stacked package of claim 1, wherein the upper chip is larger than the lower chip in size.

12. The multi-chips stacked package of claim 6, wherein the underfill further entirely covers the first active surface of the upper chip.

13. The multi-chips stacked package of claim 6, wherein the underfill further covers a portion of the upper surface of the substrate.

14. The multi-chips stacked package of claim 6, wherein the underfill further covers a portion of the lower surface of the substrate.